TDAQ Global Firmware
WBS 6.8.3

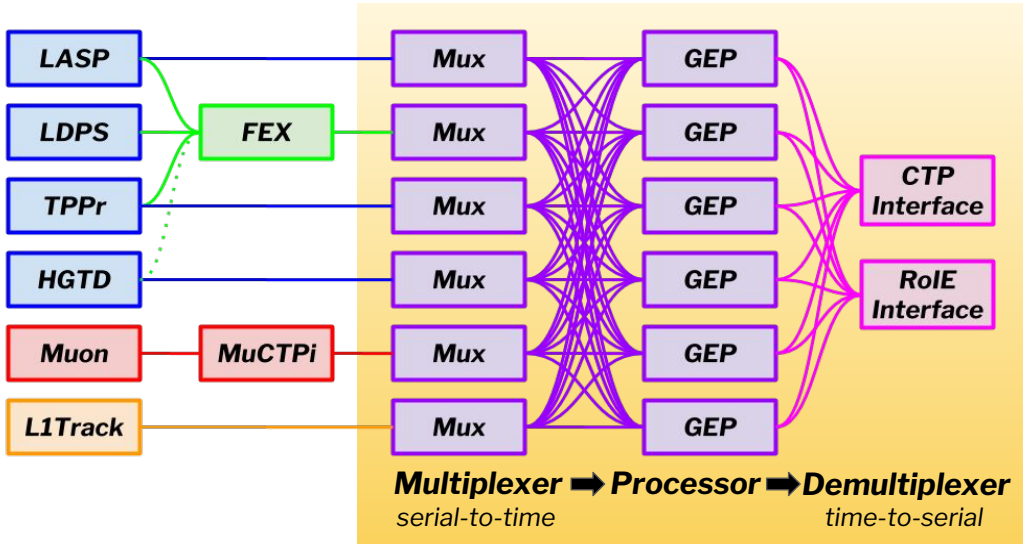
Stephanie Majewski,
University of Oregon

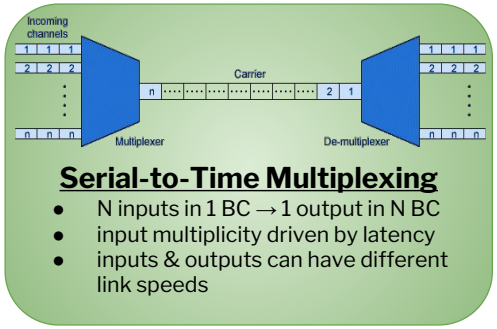
Meeting with Institute Contacts
May 12, 2017

Global Hardware Proposal (MB, DS)

Global Trigger: Time Multiplexed Architecture

- ***Data transfers are time multiplexed within the Global Trigger System***
  - increases flexibility
  - simplifies evolution
  - **maximizes physics potential**
- ***<u>Hidden</u> from external systems***
  - input serial data (per BC) are time multiplexed in Mux board
  - **Mux transports data to one of many Global Event Processors (GEP) to run trigger algorithms**
  - Global Trigger interfaces with CTP & RoIE through time-to-serial demultiplexers





Michael Begel

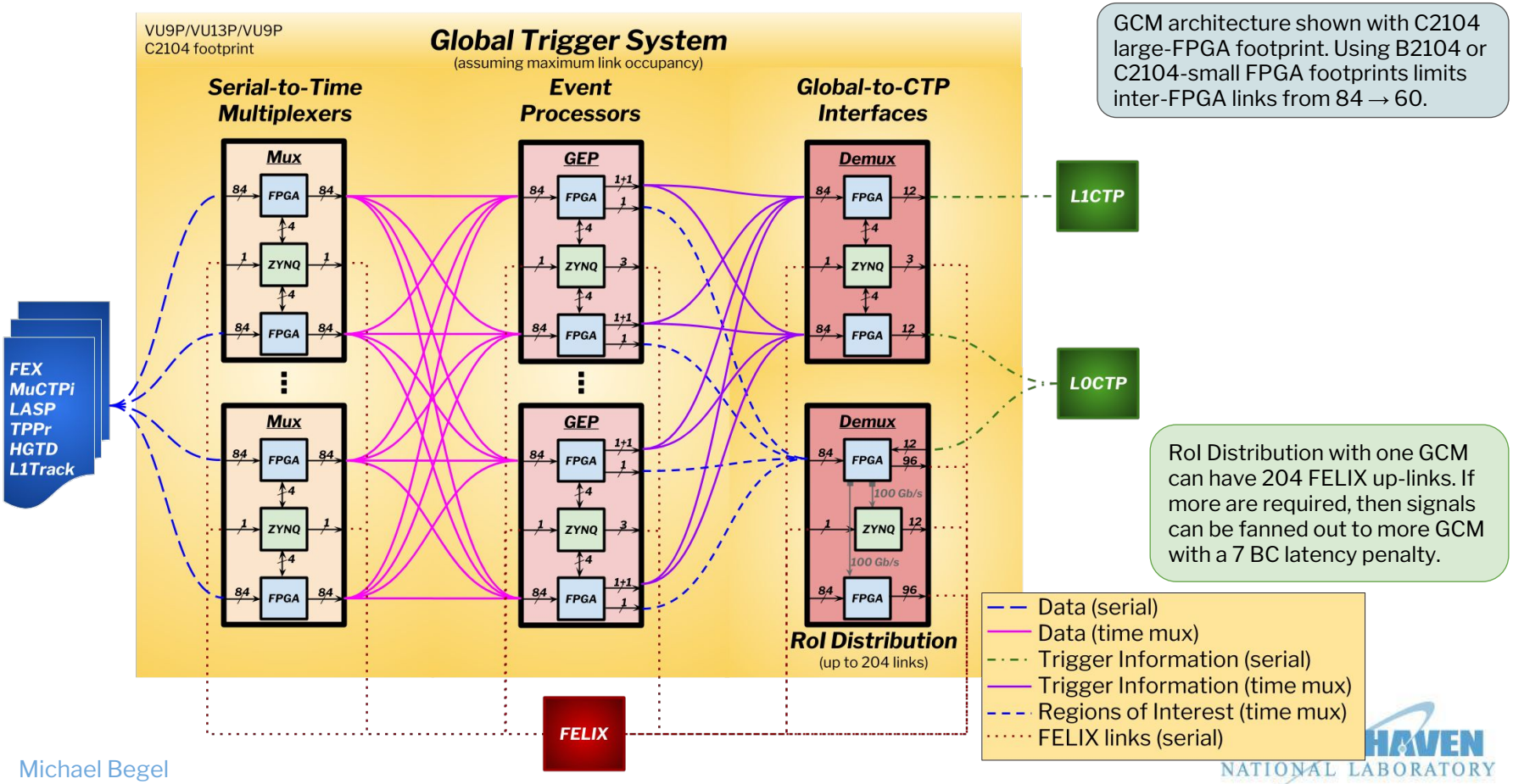
BROOKHAVEN NATIONAL LABORATORY

4

https://indico.cern.ch/event/590707/contributions/2565255/attachments/1448728/2233005/20170425_TDAQ_Global_Trigger_Introduction_1.pdf

Global Hardware Proposal (MB, DS)

Global Trigger System



GCM architecture shown with C2104 large-FPGA footprint. Using B2104 or C2104-small FPGA footprints limits inter-FPGA links from 84 → 60.

RoI Distribution with one GCM can have 204 FELIX up-links. If more are required, then signals can be fanned out to more GCM with a 7 BC latency penalty.

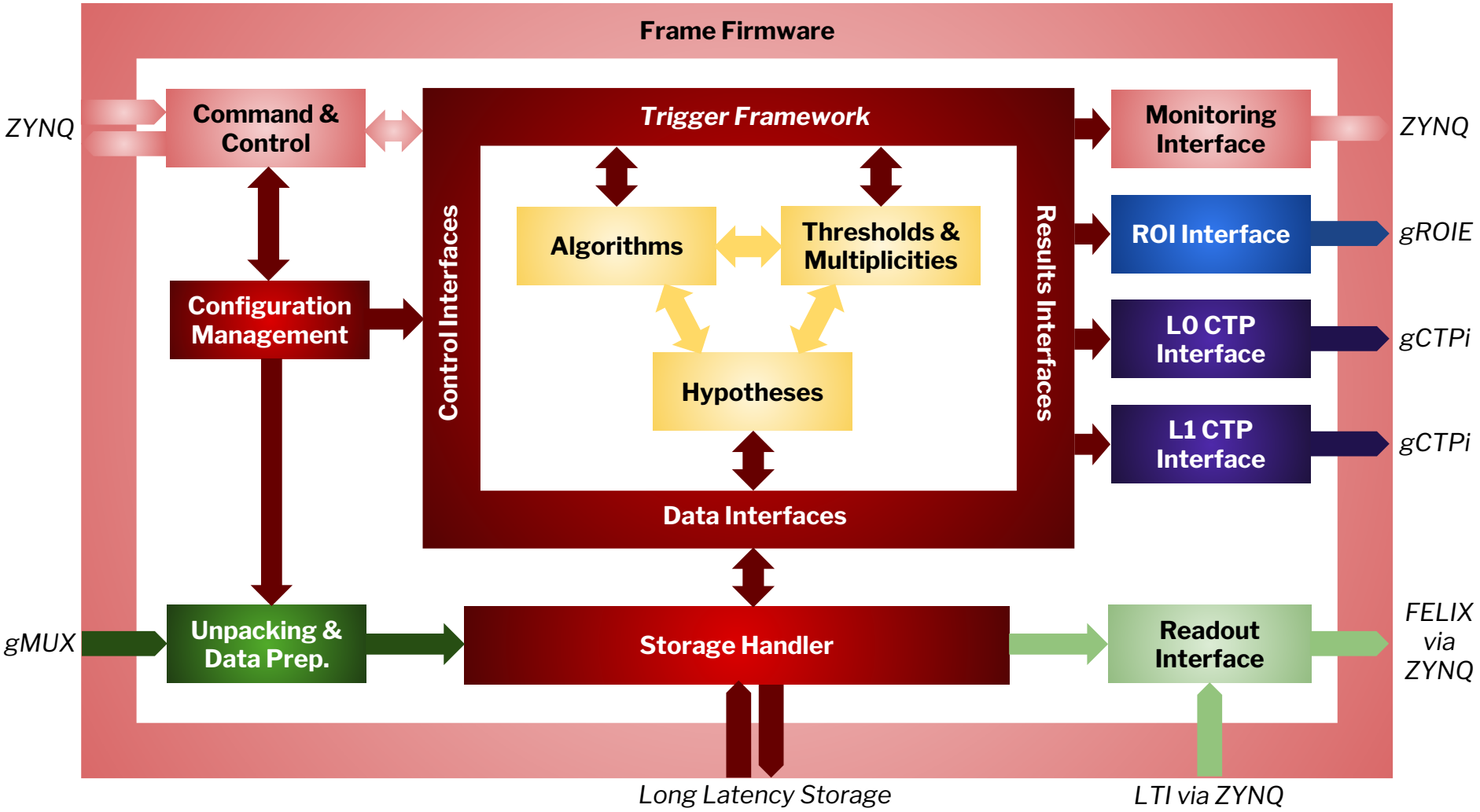
Michael Begel

BROOKHAVEN NATIONAL LABORATORY

6

https://indico.cern.ch/event/590707/contributions/2565255/attachments/1448728/2233005/20170425_TDAQ_Global_Trigger_Introduction_1.pdf

Global Firmware Proposal (MB et al)



Basis of Estimate for Firmware

Trigger Framework

WBS	Funding Agency	#FTE / year	Description	Inst.
	DOE	1.5	L0/L1 Data prep + monitoring	
	DOE	1.0	ROI Interface	
6.8.3.1	NSF	1.5	Core framework + integration	
	NSF	0.5	Algorithm interfaces + thresholds & multiplicities	
	NSF	0.5	CTP Interfaces + trigger bit assembly	
	NSF	0.5	Readout interface to FELIX	
	DOE/ NSF	2.5/3		
	TOTAL	5.5	*ATLAS core trigger software effort: 4-5 FTE / year* *L1Topo effort: 5 developers over 3 years*	

Basis of Estimate for Firmware

Trigger Framework

WBS	Funding Agency	#FTE / year	Description	Inst.
	DOE	1.5	L0/L1 Data prep + monitoring	
	DOE	1.0	ROI Interface	
6.8.3.1	NSF	1.5	Core framework + integration	MSU
	NSF	0.5	Algorithm interfaces + thresholds & multiplicities	Oregon?
	NSF	0.5	CTP Interfaces + trigger bit assembly	
	NSF	0.5	Readout interface to FELIX	Indiana?
	DOE/ NSF	2.5/3		
	TOTAL	5.5	*ATLAS core trigger software effort: 4-5 FTE / year* *L1Topo effort: 5 developers over 3 years*	

Basis of Estimate for Firmware

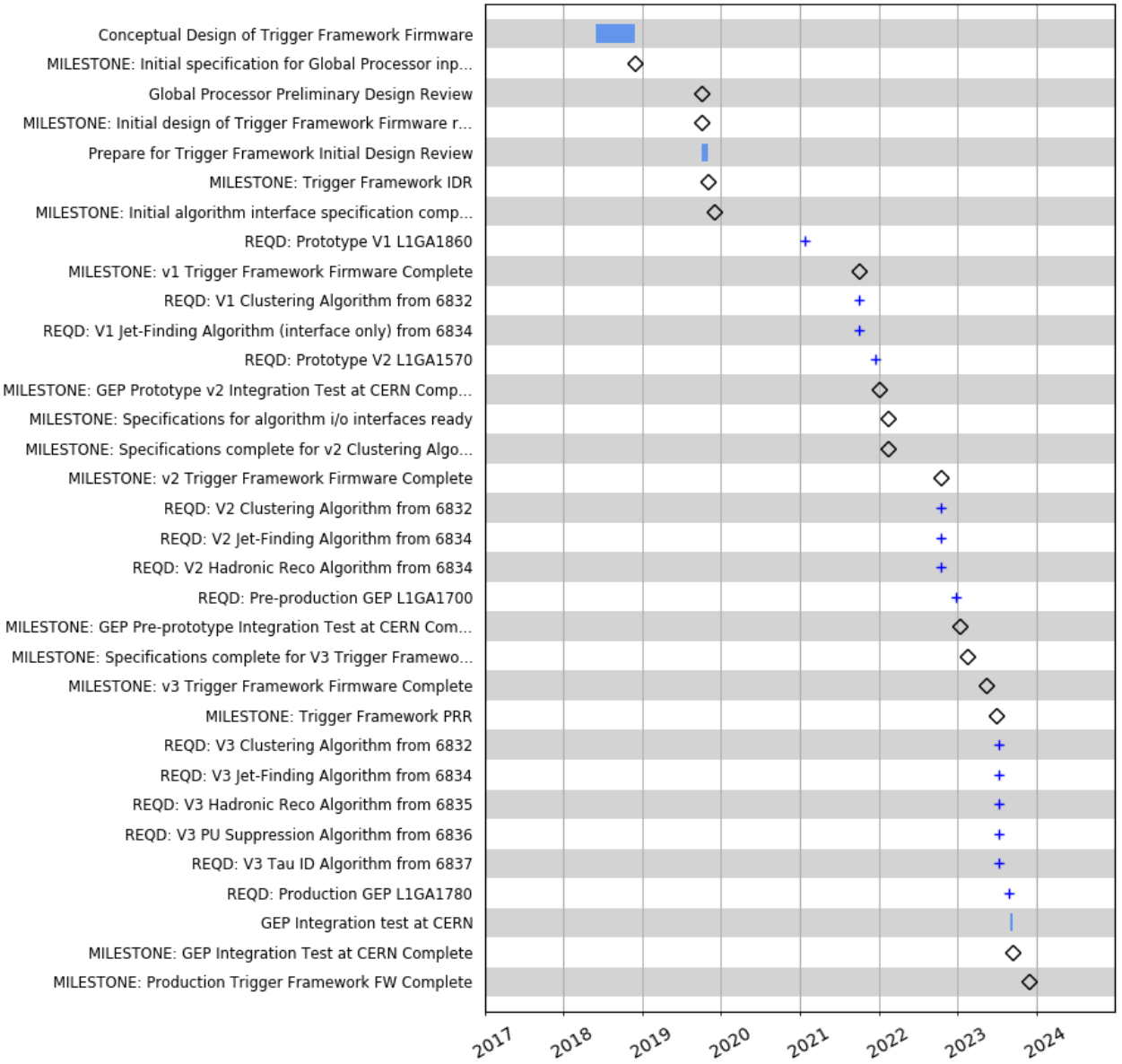
Algorithms

WBS	Funding Agency	#FTE / year	Description	Institution
6.8.3.2	NSF	0.5	Topoclustering [neighboring]	MSU
6.8.3.3	NSF	0.5	Topoclustering [data handling]	Oregon
6.8.3.4	NSF	0.5	Jet finding	Indiana
6.8.3.5	NSF	0.5	Hadronic reconstruction + boosted objects	Chicago
6.8.3.6	NSF	0.5	Pileup suppression	Pitt
6.8.3.7	NSF	0.5	Tau identification	Oregon
	TOTAL	3	*Algorithm effort based on gFEX algorithm experience*	

Task List Status

- Algorithm task lists reasonably mature / aligned
  - some scrubbing/polishing still needed!
- Trigger framework task list will likely be branched into multiple task lists → need to reach consensus on what the US can/wants to take on, and then how to divide it up
- Each algorithm integrates (links) directly with trigger framework (N→1 rather than N→N) to factorize work:
  - V1 framework: Clustering + jet-finding
  - V2 framework: Clustering, jet-finding, + hadronic reco
  - V3 framework: Clustering, jet-finding, hadronic reco, pileup suppression, tau ID
- Trigger framework (only) links to GEP hardware at integration test milestones

Trigger Framework Milestones



Global Firmware BoE (1 of 3)

	US ATLAS **HL-LHC Upgrade** **BASIS of ESTIMATE (BoE)**	**Date of Est:** 12 May 2017 **Prepared by:** **E. Lipeles, S. Majewski** **Docdb #: 43**
WBS number: 6.8.y.3	**WBS Title: Global Event Processor Firmware**	

WBS Dictionary Definition:

Global Event Processor trigger firmware, including the trigger framework and algorithm implementation for topological clustering, jet-finding, hadronic global quantity reconstruction, pileup suppression, and tau identification.

Institutes: Chicago, Indiana, MSU, Oregon, Pitt

Estimate Type (check all that apply – see BOE Report for estimate type by activity):

_X_ Analogy
___ Data Collection
___ Engineering Build-up
_X_ Expert Opinion
___ Extrapolate from Actuals
___ Parametric
___ Software Estimating

Supporting Documents (including but not limited to):

Global Firmware BoE (2 of 3)

Details of the Base Estimate (explanation of the Work)

The Global Event Processor will receive full granularity calorimeter information at 40 MHz for cells with energy above a given threshold (e.g., $|E| > 2\sigma$), and will support the reconstruction of a wide variety of trigger objects such as jets, electrons, muons, tau leptons, and event-level quantities. The system must also have "hooks" in place to evolve to a two-level architecture with inputs from Level-1 Track after a Level-0 Accept. This BoE addresses a plan for the trigger framework firmware and firmware for a selected set of trigger algorithms. The trigger framework firmware organizes the algorithms for each type of trigger and keeps track of the trigger objects needed for each algorithm. Each algorithm must be compatible with the Global Event Processor latency and resource requirements, and must be integrated into the trigger framework. This BoE includes firmware for the following algorithms:

- Topological clustering
  - an offline-like topological clustering algorithm
- Jet finding
  - an offline-like jet-finding algorithm based on topological clusters with performance similar to anti-kt
- Hadronic global object reconstruction
  - offline-like calorimeter-based MET, HT, and MHT quantities and boosted object reconstruction
- Pile-up suppression
  - dedicated calorimeter-based pileup suppression algorithms
- Tau identification
  - hadronic tau identification based on topological clusters

Global Firmware BoE (3 of 3)

Effort: The trigger framework firmware is tied to the development cycle of the Global Event Processor hardware, with an initial design phase followed by three development cycles that will each be integrated with the control firmware and tested on subsequent versions of the hardware. The algorithms will be integrated with the trigger framework firmware in stages, starting with the most resource-intensive algorithms (topological clustering and jet-finding) in v1, adding the hadronic reconstruction algorithm block in v2, and adding the integration of the remaining algorithm blocks in v3. The estimate of the effort needed for the development of the trigger framework firmware is based on the effort that was needed for firmware of similar complexity needed for the Level-1 Topological Processor currently in use in Run 2.

The algorithm effort is estimated based on experience developing the global Feature Extractor (gFEX) firmware for the Phase-I upgrade, and firmware R&D for the HL-LHC upgrade. The topological cluster algorithm block involves several complex steps, including handling the input of a much larger data volume than the gFEX experience, iterative cluster building, a weighting and calibration step, and the need to carefully manage FPGA resources. For these reasons, and based on the experience gained during R&D, it is assigned xx FTEs. The remaining algorithms are expected to have similar complexity to those developed for the gFEX, and thus are assigned xx FTEs.

Next Steps

- Task lists (w/ links) are in the project office
- BoE dictionary definition, explanation of work (through "effort" section) updated
- Action items:
  - Converge on overall basis of estimate for trigger framework
  - Decide how much scope US (NSF) can / will take on
  - Update / break out trigger framework firmware task list accordingly